Transistors based on carbon nanotubes

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***Abstract*— The applications of electronics require each day greater efficiency of the electronic devices that are used today. Among the most important aspects in production of a chip is the area occupied by the circuit: It is desired that electronic devices occupy the smallest possible space. The technology that is used today to manufacture semiconductor devices is reaching the limits, where it is increasingly difficult to obtain reduction in size without affecting other features of the device. This document shows a bibliographical review on nanotechnology, in order to present a research proposal to implement transistors based on carbon nanotubes.**

Keywords—component; carbon nanotubes; field-effect transistors;

I. INTRODUCTION

In the present article a bibliographic review of the carbon nanotube is shown, in the framework of its properties, who and how they discovered them, their current applications and the potential future applications, especially in electronics. Additionally, a work proposal is enunciated to implement transistors based on this technology: It is provided that by 2025 graphene will replace silicon, allowing the rapid miniaturization of electronic components and production of new chips [1].

II. ESTATE OF THE ART

Carbon nanotubes (also known as CNTs) are an allotrope of carbon, they have the form of cylindrical carbon molecules and have singular physics properties that make it attractive for the researcher, like mechanical strength, high electrical conductivity, and other properties.

The structure of CNT can be formed by one single or multiple wall of carbon nanotubes. The Single Wall Nanotube (SWNT) is formed by winding a layer of graphite wrapped up to form a seamless tube with a thickness of 1 single carbon atom and have typically a diameter of 1 - 2 nm and a length of several micrometers. The aspect ratio of these nanotubes is considered ideally nearly one-dimensional material, and as such the SWCNTs are expected to have all the unique properties predicted for these low-dimensional structures. [2]

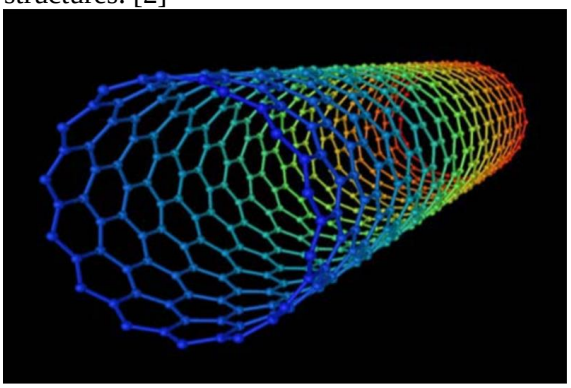

Figure 1: Single walled carbon nanotube

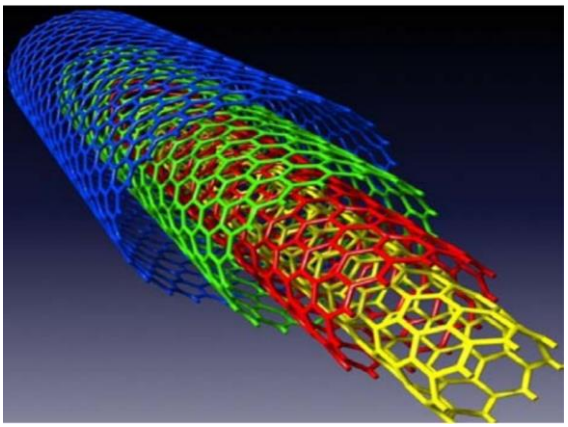

Figure 2: Multi walled carbon nanotube

The double wall nanotube (DWNT) [3] have two atoms of thickness and the graphite multiple wall nanotube (MWNT) contents several sheets (rolled into themselves; also known by the names "Buckyball or Fullereno", thanks to engineer and architect Buckminster Fuller, who worked on the creation of geodesic domes that is precisely the geometrical form of a icosahedron. These MWNT are the strongest carbon fibers that are known, and they have very interesting properties: tensile strength of 45 billion pascals, a capacity of current transport estimated in one billion amperes per square centimeter at room temperature and a thermal stability of

2,800 degrees Celsius in vacuum, and 750 degrees Celsius in the air. On the other hand, the electrical properties of multi-walled nanotubes (MWCNTs) have received less consideration because of their complex structure: every carbon shell can have different electronic character and chirality and the presence of shell–shell interactions modify the global behaviour.

The first carbon nanotubes were synthesized from hollow carbon molecules by Sumio Iijima in 1991. Later in 1993 two groups discover the single wall carbon and some methods to produce them using transition-metal catalysts: Sumio Iijima with his group at NEC and D. S. Bethune at IBM. [4] [5].

III. METHOS OF SYNTHETIZING CNTS

They are obtained and characterized by four methods: The first is the so-called "electric arc discharge" method, which allows the manufacture of macroscopic quantities of nanotubes. It consists on connecting two graphite rods to a power supply, these are separated by a few millimeters and then a current across the bars is forced. By generating a spark of around hundreds of amperes of intensity, the carbon evaporates into a hot plasma. Part of this plasma condensate in form of single and multi-walled carbon nanotubes. This method was developed and published in 1992, by Thomas Ebbeser and Pullickel M. Ajayan, from the Fundamental Research Laboratory of NEC. [6]

The second method is called "Chemical Vapor Deposition" (CVD) [7],which was introduced by Morinubo Endo, of the University of Shinshu in Nagano (Japan). In this method, a substrate is placed in an oven and heated up to 600°C. Then methane and other gases are slowly added, releasing carbon atoms, which can recombine in form of nanotubes. It allows the controlled synthesis, that is, number of walls, length and microscopic structure of SWNTs, DWNTs and MWNTs with purity up to 98%. This method requires a suitable substrate often impregnated with the catalyst on which the growth of the CNTs occurs. The more common substrates are generally Si, SiO2 (Quartz), Al2O3 or MgO. In addition to this, the impurities involved in the process are usually: Metals and inorganic oxides coming from the catalyst and amorphous Carbon.

The third method is known as "laser ablation" [8]. In this technique a mixture of carbon and transition metals are vaporized by a laser intruding on a metal-graphite composite target bar. Intense pulses of laser beam are focused to a 6-7 mm diameter spot of the metal-graphite bar. In the reactor, the temperatures are elevated and surrounded by the presence of an inert gas. The soot produced by the laser vaporization was swept by the flowing Ar gas from the high-temperature zone and deposited onto a water-cooled copper collector. The nanotubes obtained are single-walled with a range of diameters that can be controlled by varying the reaction temperature. It is a method with a good performance, but it is very expensive since it requires high power lasers.

The fourth and last presented method is known as "plasma torch" and is developed specially to synthetize single-wall carbon nanotubes [9]. It was patented by Olivier Smiljanic on the 2009 [10]. This method is based on the atomization of a gaseous mixture by an atmospheric-pressure microwave plasma torch. Microwaves are generated by a magnetron from a domestic microwave oven supplied by a DC current. The microwave radiation travels inside a copper waveguide, which is short-circuited at one end by a metallic plate. A boron nitride or quartz tube serves as the `plasma tube' and traverses the waveguide at a position a quarter wavelength upstream from the short-circuit. The plasma flame is sustained by the microwave radiation and confined inside the plasma tube. It is kept from attaching to the walls by a swirl jet of argon. The carbon-containing ethylene gas and the catalyst in the form of ferrocene are introduced by an axial flow. Ferrocene vapor obtained by a temperature-controlled sublimation is entrained by an inert gas (argon). [9]

These above-mentioned methods have advantages and limitations: In the Electric Arc Discharge Method, the high temperatures and metal catalysts added to the bars can produce single and multiple wall nanotubes but with few structural defects. Also, the nanotubes tend to be short (50 microns or less) and to be deposited in random shapes and sizes, which is not desired in nanoelectronics. The Chemical Vapor Deposition (CVD) method is the simplest to make long nanotubes, useful in the nano-fibers employed in composite materials. The restriction for the usage in electronics is that the nanotubes produced are usually multiple-walled and frequently plagued with defects. The laser ablation method produces single-walled nanotubes with a range of diameters that can be controlled by varying the reaction temperature, but it needs very expensive and accurate lasers devices. In comparison of the previous presented techniques, the plasma torch method is continuous and easily scalable, and therefore suitable for large-scale commercial production of SWNT. This apparently solve the problems of cost and availability of sufficiently large

quantities of SWNT which were the main issues of the previous presented techniques: laser ablation and arc discharge techniques.

IV. TRANSISTORS IN ELECTRONICS

The miniaturization has played always a key role in electronic evolution with a continuous decrease in the size of silicon transistors in the recent decades, reducing the cost of electronics and leading to higher processing power with lower energy consumption. Since decades nanophysics and engineers are working on developing faster transistors, smaller or with less power consumption.

But an already known problem occurs by scaling down the conventional CMOS technology. This until now unceasing reduction of the size of a single transistor will be stop at 7nm. While 7nm nodes are technically possible to produce with silicon, after that size some problems appear, where silicon electrons become so physically close together that they experience the quantum tunnelling effect. The already know problem of the scaling limit of conventional CMOS, should be in the coming future be solved by the carbon nanotube technologies [13].

As the transistors get smaller, it is more difficult to control the way electrons move through the silicon channel to turn the transistor on and off. A solution to this problem have solved Intel, for example, by developing the first 3D Tri-Gate 22 nm transistor for mass production in 2012 [14]. Despite this, the future of small switching technologies carbon nanotubes technology will be a replacement for silicon technology.

A. Carbon nanotube field effect transistors

Carbon nanotube transistors are the promising technology to obtain sub-7 nm channel lengths transistors and continue the fulfilment of the Moore's law. From the various transistor types, FETs, particularly in CMOS form, have been proven to be the most technologically useful device structures in electronics. Analogy, carbon nanotube transistors have been developed using this CMOS technology and they are named in fact CNTFET in similarity to the silicon field effect transistor. CNTFETs represent an emerging technology to extend and/or complement the traditional Silicon MOSFET.
The carbon nanotube field-effect transistors were demonstrated at the university of Delf by Dekker's group and Avouris's group at IBM in 1998. [15]

The Figure 3 shows an early prototype of a CNTFETs fabricated with a single wall nanotube (SWCNT). Two noble metal electrodes prefabricated by lithography were used as source and drain, the carbon nanotube was used as a channel and the heavily doped wafer as a gate. The transistor was built over an oxidized silicon wafer and made by inserting a semiconductor a SWCNT between the source and drain in field effect transistors (FET), to create a "highway" for the circulation of electrons. Single-wall semiconducting tubes (SWCNTs) are best suited for CNTFETs because their electron system is not bypassed by inner shells.

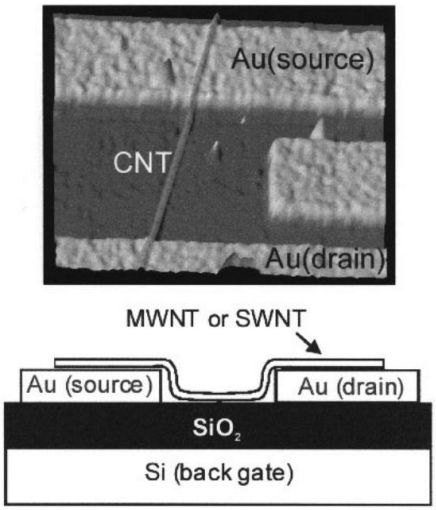

Figure 3: early carbon nanotube transistor. Bottom: Schematic cross section of the CNTFET [16]

The current between source and drain can be activated, or deactivated, by applying a small voltage to the gate, which causes the conductivity of the nanotube to change by a factor greater than 10^6, comparable to the silicon FET. As a result, CNTFETs would switch without error and consume less energy than a silicon device. In addition, switching speeds can reach terahertz, which means switching 10^4 times faster than current processors.

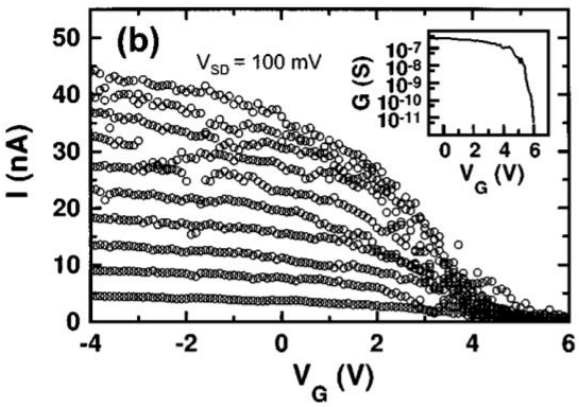

Figure 4: I –V_G curves for V_SD = 10– 100 mV in steps of 10 mV. The inset shows that the gate modulates the conductance by 5 orders of magnitude (V_SD = 10 mV)

In 2016 investigators of the University of Wisconsin-Madison created the first carbon nanotube transistors that outperform state-of-the-art of silicon transistors [17] [18]. I think important to remark that the mentioned paper was published as open source. This transistor approach adopts an array of densely packed carbon nanotube for the channel instead of one single as it was. The CNTs are deposited onto Silicon wafers with 15 nm of SiO_2, which yields dense arrays of CNTs that remain isolated.

The SiO_2 is employed as a FET back-gate dielectric and the Si substrate is used as gate electrode. The source and drain electrodes consist of 30-nm-thick layers of Palladium. The channel width is 4µm and the length varies from 95 to 340 nm.

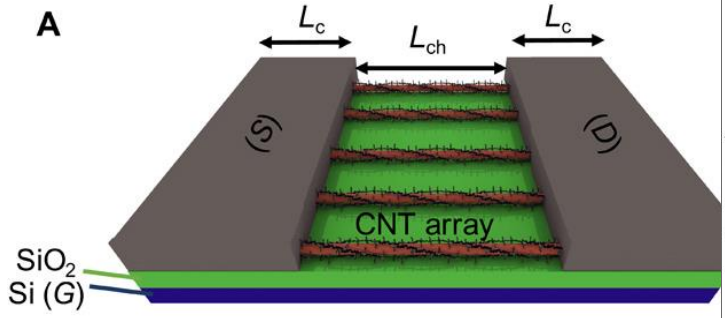

Figure 5: Schematic of CNT array sitting on a SiO2/Si back gate (G) with top Pd source (S) and drain (D) electrodes. [18]

The characteristic curve of the CNT arrays can be seen on the Figure 6. This transistor approach in the format of an array in which quasi-ballistic transport is simultaneously driven through many, tightly packed CNTs in parallel, noticeably improving the absolute current drive of the silicon FETs. This performance is achieved due to the combined excellent alignment and spacing of the CNTs, some postdeposition treatment on the CNTs and the high electronic-type purity of the semiconducting CNTs.

With this transistor the performance of the outstand the state-of-the-art Si MOSFETs for the first time, when compared at an equivalent gate oxide thickness and at the same off-state current density, as shown in the Figure 7.

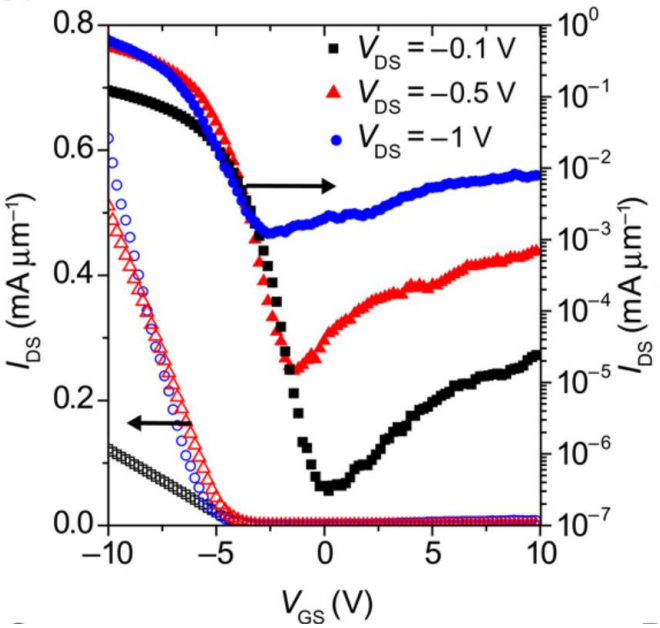

Figure 6: IDS-VGS curves forward sweep for a FET with Lch = 100 nm where the open and filled symbols are plotted on linear and logarithmic scales, respectively. [18]

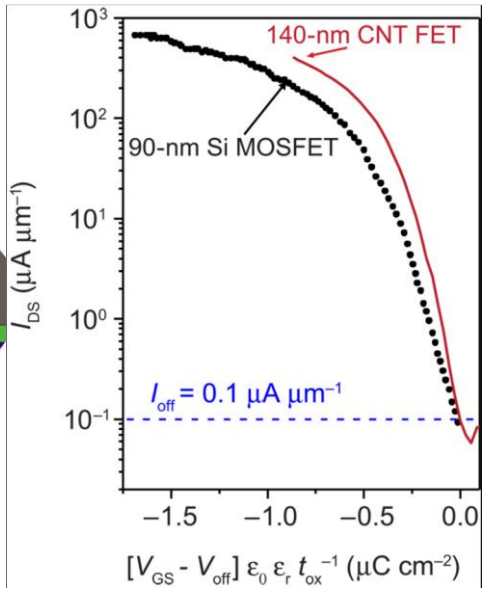

Figure 7: Benchmarking CNT array FET performance against Si MOSFETs [18]

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